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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,794	11/21/2003	Lorenzo Di Gregorio	068758.0146	3086

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EXAMINER	
LAI, VINCENT	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,794	DI GREGORIO ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Fritz M. Fleming

Supervisory FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
AU 2181

3/13/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/21/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copies of the priority documents have been received.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 11/21/2003 was considered by the examiner.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Device and Method for Controlling Processing of Data Elements of a Data Stream Utilizing a Multitude of Units with Specific Functions.

4. The disclosure is objected to because of the following informalities: On page 18, line 10, it appears an error was made in typing "If."

Appropriate correction is required.

Claim Objections

5. Claims 1-37 are objected to because of the following informalities:

Claims 1-5 all lack antecedent basis but the lack of antecedent basis is not such that the claims are not interpretable.

In claim 1, lines 4 and 5, the term "the context" is used without antecedent basis. It is suggested to be changed to "context."

Also in claim 1, line 8, the term "the sequence" is used without antecedent basis. It is suggested to be changed to "a sequence."

In claim 2, line 3, the term "the sequence" is used without antecedent basis. It is suggested that above change be made or it to be changed to "a sequence."

In claim 3, line 2 and 4, the term "the increment" is used without antecedent basis. It is suggested to be changed to "an increment."

In claim 4, line 2, the term "the context" is used without antecedent basis. It is suggested to be changed to "a context."

Also in claim 4, line 3, the term "the preceding data elements" is used without antecedent basis. It is suggested to be changed to "preceding data elements."

In claim 5, line 2, the term "the activated context" is used without antecedent basis. It is suggested to be changed to "an activated context."

Claim 9 states "the repetitions are interrupted at the value 0." The statement is suggested to be changed to "the repetitions are interrupted by the value 0."

Claim 10 uses a comma in line 4 that is unnecessary and is suggested to be deleted.

Claims 20-24 all lack antecedent basis but the lack of antecedent basis is not such that the claims are not interpretable.

In claim 20, line 5, the term "the context" is used without antecedent basis. It is suggested to be changed to "context."

Also in claim 20, line 7, the term "the sequence" is used without antecedent basis. It is suggested to be changed to "a sequence."

In claim 21, line 3, the term "the sequence" is used without antecedent basis. It is suggested that above change be made or it to be changed to "a sequence."

In claim 22, line 2 and 4, the term "the increment" is used without antecedent basis. It is suggested to be changed to "an increment."

In claim 23, line 2, the term "the context" is used without antecedent basis. It is suggested to be changed to "a context."

Also in claim 23, line 3, the term "the preceding data elements" is used without antecedent basis. It is suggested to be changed to "preceding data elements."

In claim 24, line 2, the term "the activated context" is used without antecedent basis. It is suggested to be changed to "an activated context."

Claim 28 states "the repetitions are interrupted at the value 0." The statement is suggested to be changed to "the repetitions are interrupted by the value 0."

Claim 29 uses a comma in line 4 that is unnecessary and is suggested to be deleted.

All other claims are objected to because of dependences to above-mentioned claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-37 are rejected to under 35 U.S.C. 112, second paragraph because of the following informalities:

Claims 1 and 20 recites the limitation "the instruction " in lines 10-11, and 8, respectively. There is insufficient antecedent basis for this limitation in the claim. It is unclear as to which fetched instruction the limitation “the instruction” in lines 10-11, and 8 of claim 1 and 20, respectively.

Claims 5, and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear as to what "it" of line 6 for both claims refers to.

All other claims are rejected to because of dependences to above-mentioned claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-18, and 20-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Shintani et al (U.S. Patent # 5,721,865), herein referred to as Shintani et al.

As per claim 1, Shintani et al discloses a device for controlling processing of data elements, in which a thread is assigned to each data element (See column 8, lines 5-11: A thread is assigned according to the control information) and no more than one data element enters the device at one time (See column 31, lines 28-30: An interval set in between data elements discloses that only one data element can enter a device at a time), comprising:

a first unit (Prefetch unit 105, see figure 1 and 2), in which the context for each thread is entered (See column 8, lines 5-11: The instruction is fetched according to control information that is set, whereas a thread is viewed as collection of instructions), and which fetches an instruction during a first clock cycle that is entered in the context of the thread assigned to the incoming data element (See column 8, lines 5-11: Is a normal prefetch),

a second unit (Instruction fetch circuit 1101A, see figure 1 and 11), which, during a second clock cycle, fetches an instruction (See column 11, lines 52-55: Is a normal fetch), which succeeds a stipulated instruction in the sequence of instructions of a stipulated thread (See column 12, lines 17-26: This is normal operation when a prefetch unit is available and is described further by Shintani et al in the lines cited), and

a third unit (Instruction decoder 1101B, see figure 1, and 11), which, during the second clock cycle (See column 41, lines 59-61: Shintani et al discloses a pipeline which embodies the three units connected. A decode during a second clock cycle is normal since a fetch is normally done during a first clock cycle), decodes (See column 11, lines 52-55: Decoding is done) the instruction that is provided for processing of the data element and fetches a control signal for processing of the data element (See column 11, line 66-column 12, line 16: Control signals are sent out according to a decoded signal).

As per claim 2, Shintani et al discloses wherein

the instruction fetched by the second unit is the instruction, whose position in the sequence of instructions of the stipulated thread, is the increment of the position of the stipulated instruction (See column 12, lines 17-24: After the prefetch instruction, the next instruction comes from the general register, which holds fetched instructions from the normal instruction fetcher).

As per claim 3, Shintani et al discloses wherein

the second unit is fed with the increment of a count value (Base register number BRN, see column 12, lines 3-8) and an identification value, which designates a thread, (Decoded information LD, see column 12, lines 3-8) and

the second unit, by means of the increment and the identification value, determines the instruction which assumes in the thread designated by the identification value the position designated by the increment assumes (See column 12, lines 3-16: The device acts accordingly to the control data that is given to it).

As per claim 4, Shintani et al discloses wherein the first unit activates the context of the thread assigned to the incoming data element, if the preceding data element refers to another thread (See column 14, lines 57-59, and column 19, lines 38-40: Context switching is allowed and is called by prefetch controls).

As per claim 5, Shintani et al discloses wherein

the first unit fetches an instruction of the thread stated in the activated context and transmits this instruction, which is the first instruction of the thread, in particular, to the third unit for decoding (See figure 1, 2, and 11: There is no decoder in the prefetch unit but there is a connection from the prefetch unit to the processor, which does have a decoder and thus in order to fully decode an instruction, a prefetched instruction must be passed onto the decoder),

the first unit transmits the increment of the position that the instruction fetched by it assumes in the thread, to the second unit (See column 12, lines 3-16: The device acts accordingly to the control data that is given to it).

As per claim 6, Shintani et al discloses wherein the second unit determines the instruction that succeeds the instruction fetched by the first unit in the thread (See column 12, lines 17-24: This can be determined from the control signals that are passed).

As per claim 7, Shintani et al discloses wherein for data elements entering the device in succession, the same thread is assigned, as long as the same instruction is used, until a stipulated condition is met (See column 19, lines 38-40: A context switch is necessary when a stipulated condition is met otherwise context remains unchanged and thus the same thread is assigned).

As per claim 8, Shintani et al discloses wherein repetition of an instruction is accomplished by the fetching of the same control signal by the third unit (See column 43, lines 25-28: Fetching can be skipped in a loop and thus the next step would be decoding).

As per claim 9, Shintani et al discloses wherein

the number of repetitions of an instruction is stipulated by a value (Loop length, see column 41, lines 21-22), this value, during a repetition of the instruction, is decremented by the third unit (The decrement of the value is not explicitly discloses but is inherent to a loop operation and since fetching is already established as being skipped when a loop is run, decrement must be done in the third unit), and

the repetitions are interrupted at the value 0 (This is the natural course of when a loop ends).

As per claim 10, Shintani et al discloses wherein after fulfillment of the stipulated condition for processing of the data element entering the device next, a stipulated instruction within the thread is used, if the same thread is assigned to this data element (See column 19, lines 38-40: A context switch is necessary when a stipulated condition is met otherwise context remains unchanged and thus the same thread is assigned).

As per claim 11, Shintani et al discloses wherein the inquiry into fulfillment of the stipulated condition occurs in the third unit (See column 14, lines 57-59: Since context

switches are decided after checking the general purpose register, it means instructions have already been fetched and thus it must be done in the third unit).

As per claim 12, Shintani et al discloses wherein the stipulated instruction is the instruction fetched by the second unit (See column 12, lines 17-24: After the prefetch instruction, the next instruction comes from the general register, which holds fetched instructions from the normal instruction fetcher).

As per claim 13, Shintani et al discloses further comprising: a connection line for data transmission between the second unit and the third unit (See figure 11, the two units are contained within one unit and thus are connected), through which the instruction, fetched by the second unit is transmitted to the third unit (See figure 11 and column 11, lines 52-55: The decoder decodes instructions from the instruction fetch circuit or the request control unit).

As per claim 14, Shintani et al discloses wherein the instruction fetched by the second unit is transmitted to the first unit and entered in the context there (See column 8, lines 24-29: Done with prefetch control information).

As per claim 15, Shintani et al discloses wherein the stipulated instruction is fetched by the first unit and transmitted to the third unit for decoding (See figure 1, 2, and 11: There is no decoder in the prefetch unit but there is a connection from the

prefetch unit to the processor, which does have a decoder and thus in order to fully decode an instruction, a prefetched instruction must be passed onto the decoder).

As per claim 16, Shintani et al discloses wherein the third unit, after fulfillment of the stipulated condition, transmits an instruction to the first unit as to which instruction is to be fetched (See column 39, lines 37-45: Once a loop ends, a prefetch request is made with a load instruction).

As per claim 17, Shintani et al discloses wherein the stipulated condition, whose fulfillment leads to interruption of repetitions of an instruction, is fulfilled by a signal controllable from outside of device (See column 37, lines 7-9: An interrupt signal can end a loop), or by a specific data element entering the device (See column 35, lines 33-35: Once a certain condition is met, a wait loop will end), or by a specific state of the corresponding thread (See column 39, lines 37-45: A loop can end when its execution changes state when a certain condition is met), or by a specific instruction to processed (See column 37, lines 7-9: An interrupt signal or instruction can end a loop).

As per claim 18, Shintani et al discloses further comprising: a program memory (Memory 1, see figure 1), in which the instructions for processing of the data elements are entered (See column 1, lines 48-53: Instructions are read from memory and thus are entered in memory), and in which information is entered for each instruction on how many data elements the instruction is to be applied (See column 1, lines 53-57: The

prefetch instruction reads out data locations and thus the number of data elements applied would be known), wherein the program memory has program lines, in particular, in which one instruction and the corresponding information, with reference to the number of repetitions, are entered (See column 41, lines 21-22: Loop length is one of the arguments in an instruction).

As per claim 20, Shintani et al discloses a method for controlling processing of data elements, comprising the steps of:

assigning a thread to each data element (See column 8, lines 5-11: A thread is assigned according to the control information) and no more than one data element enters the device at one time (See column 31, lines 28-30: An interval set in between data elements discloses that only one data element can enter a device at a time),

fetching (See column 8, lines 5-11: The instruction is fetched according to control information that is set) an instruction in a first unit during a first clock cycle that is entered in the context of the thread assigned to the incoming data element (See column 11, lines 52-55: Is a normal fetch),

fetching (See column 11, lines 52-55: Is a normal fetch) an instruction in a second unit, which succeeds a stipulated instruction in the sequence of instructions of a stipulated thread (See column 12, lines 17-26: This is normal operation when a prefetch unit is available and is described further by Shintani et al in the lines cited), and

decoding (See column 11, lines 52-55: Decoding is done) the instruction that is provided for processing of the data element and fetching a control signal for processing

of the data element in a third unit (See column 11, line 66- column 12, line 16: Control signals are sent out according to a decoded signal).

As per claim 21, Shintani et al discloses wherein the instruction which succeeds the stipulated instruction is the instruction, whose position in the sequence of instructions of the stipulated thread, is the increment of the position of the stipulated instruction (See column 12, lines 17-24: After the prefetch instruction, the next instruction comes from the general register, which holds fetched instructions from the normal instruction fetcher).

As per claim 22, Shintani et al discloses wherein

Feeding the second unit with the increment of a count value (Base register number BRN, see column 12, lines 3-8) and an identification value, which designates a thread, (Decoded information LD, see column 12, lines 3-8) and

the second unit, by means of the increment and the identification value, determines the instruction which in the thread designated by the identification value assumes the position designated by the increment (See column 12, lines 3-16: The device acts accordingly to the control data that is given to it).

As per claim 23, Shintani et al discloses wherein activating the context of the thread assigned to the incoming data element by the first unit, if the preceding data

element refers to another thread (See column 14, lines 57-59, and column 19, lines 38-40: Context switching is allowed and is called by prefetch controls).

As per claim 24, Shintani et al discloses wherein

Fetching an instruction of the thread stated in the activated context and transmitting this instruction by the first unit, which is the first instruction of the thread, in particular, to the third unit for decoding (See figure 1, 2, and 11: There is no decoder in the prefetch unit but there is a connection from the prefetch unit to the processor, which does have a decoder and thus in order to fully decode an instruction, a prefetched instruction must be passed onto the decoder),

transmitting the increment of the position that the instruction fetched by it assumes in the thread, to the second unit (See column 12, lines 3-16: The device acts accordingly to the control data that is given to it).

As per claim 25, Shintani et al discloses wherein determining the instruction that succeeds the instruction fetched by the first unit in the thread (See column 12, lines 17-24: This can be determined from the control signals that are passed).

As per claim 26, Shintani et al discloses wherein assigning the same thread for data elements entering in succession as long as the same instruction is used, until a stipulated condition is met (See column 19, lines 38-40: A context switch is necessary

when a stipulated condition is met otherwise context remains unchanged and thus the same thread is assigned).

As per claim 27, Shintani et al discloses wherein repetition of an instruction is accomplished by the fetching of the same control signal by the third unit (See column 43, lines 25-28: Fetching can be skipped in a loop and thus the next step would be decoding).

As per claim 28, Shintani et al discloses wherein

the number of repetitions of an instruction is stipulated by a value (Loop length, see column 41, lines 21-22),

this value, during a repetition of the instruction, is decremented by the third unit (The decrement of the value is not explicitly discloses but is inherent to a loop operation and since fetching is already established as being skipped when a loop is run, decrement must be done in the third unit), and

the repetitions are interrupted at the value 0 (This is the natural course of when a loop ends).

As per claim 29, Shintani et al discloses wherein after fulfillment of the stipulated condition for processing of the data element entering the device next, a stipulated instruction within the thread is used, if the same thread is assigned to this data element

(See column 19, lines 38-40: A context switch is necessary when a stipulated condition is met otherwise context remains unchanged and thus the same thread is assigned).

As per claim 30, Shintani et al discloses wherein the inquiry into fulfillment of the stipulated condition occurs in the third unit (See column 14, lines 57-59: Since context switches are decided after checking the general purpose register, it means instructions have already been fetched and thus it must be done in the third unit).

As per claim 31, Shintani et al discloses wherein the stipulated instruction is the instruction fetched by the second unit (See column 12, lines 17-24: After the prefetch instruction, the next instruction comes from the general register, which holds fetched instructions from the normal instruction fetcher).

As per claim 32, Shintani et al discloses wherein the instruction fetched by the second unit is transmitted to the first unit and entered in the context there (See column 8, lines 24-29: Done with prefetch control information).

As per claim 33, Shintani et al discloses wherein the stipulated instruction is fetched by the first unit and transmitted to the third unit for decoding (See figure 1, 2, and 11: There is no decoder in the prefetch unit but there is a connection from the prefetch unit to the processor, which does have a decoder and thus in order to fully decode an instruction, a prefetched instruction must be passed onto the decoder).

As per claim 34, Shintani et al discloses wherein after fulfillment of the stipulated condition, transmitting an instruction by the third unit to the first unit as to which instruction is to be fetched (See column 39, lines 37-45: Once a loop ends, a prefetch request is made with a load instruction).

As per claim 35, Shintani et al discloses wherein the stipulated condition, whose fulfillment leads to interruption of repetitions of an instruction, is fulfilled by a signal controllable from outside of device, or by a specific data element entering the device, or by a specific state of the corresponding thread, or by a specific instruction to processed (See column 39, lines 37-45: Once a loop ends, control signals that are passed to other parts of the device).

As per claim 36, Shintani et al discloses further comprising: entering (See column 1, lines 48-53: Instructions are read from memory and thus are entered in memory) the instructions for processing of data elements into a program memory, wherein information is entered for each instruction on how many data elements the instruction is to be applied (See column 1, lines 53-57: The prefetch instruction reads out data locations and thus the number of data elements applied would be known), wherein the program memory has program lines, in particular, in which one instruction and the corresponding information, with reference to the number of repetitions, are entered (See column 41, lines 21-22: Loop length is one of the arguments in an instruction).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 19 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shintani et al (U.S. Patent # 5,721,865), herein referred to as Shintani et al in view of Shimazaki et al (U.S. Patent # 5,483,552), herein referred to as Shimazaki et al.

In claim 19, Shintani et al teaches the devices as claimed in claim 1 (See the 35 USC 102b rejection of claim 1).

Shintani does not teach a delay unit.

Shimazaki et al does teach a two series-connected delay units that delay the data element by one clock cycle each (See column 5, lines 42-45: There are two delay units connected in series and delays any amount of time, including one clock cycle).

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Shintani et al to include a delay unit because a delay unit allows for delaying the use of data and thus ensures that data is received is proper (or equalized) (See Shimazaki et al column 4, lines 26-30), since data propagation may be delayed due to numerous reasons well known to a person having ordinary skill in the art at the time of the invention. This improvement would lead

to greater reliability and more likelihood that the prefetched data will be ready for use when it is needed.

In claim 37, Shintani et al teaches the method as claimed in claim 20 (See the 35 USC 102b rejection of claim 1).

Shintani does not teach the method of delaying.

Shimazaki et al does teach delaying the data element by two clock cycles. (See column 5, lines 42-45: There are two delay units connected in series which may delay any amount of time, including two clock cycle).

It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to have modified Shintani et al to include a method to delay because a method to delay allows for the proper reception of inputs (See Shimazaki et al column 4, lines 26-30), and this improvement would lead to greater reliability and more likelihood that the prefetched data will be ready for use when it is needed.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following are cited to show a device and method for controlling processing of data elements of a data stream utilizing a multitude of units with specific functions:

U.S. Patent # 3,418,638 to Anderson et al shows instruction processing unit for

program branches.

US 2004/0075747 A1 to Silverbrook shows a monolithic integrated circuit having a number of programmable processing elements.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

vl
March 6, 2006

Supervisory

Fritz M. Fleming
FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
2181
3/13/2006